What is claimed is:

1. A boosting circuit, comprising:

a reference voltage generating circuit unit for generating a reference voltage according to an address transition detection signal that is delayed by a given time;

a first boosting means for outputting a given boosting voltage according to the address transition detection signal and an inverted signal thereof;

a sensing circuit for sensing a flash memory cell according to the reference voltage and the boosting voltage of the first boosting means, wherein the output signal of the sensing circuit is changed depending on the boosting voltage of the first boosting means applied to a gate terminal of the flash memory cell;

a switching circuit for applying the boosting voltage of the first boosting circuit or the power supply voltage depending on the boosting voltage of the first boosting circuit and the output signal of the sensing circuit; and

a second boosting means for supplying the power supply voltage to an output terminal according to the address transition detection signal, wherein the second boosting means is boosted according to the boosting voltage of the first boosting circuit or the power supply voltage to output the boosting voltages of two levels to the output terminal.

2. The boosting circuit as claimed in claim 1, wherein the reference voltage generating circuit unit comprises:

an address transition detection signal delay circuit for delaying the address transition detection signal by a given time; and

a reference voltage generating circuit for generating the reference voltage according to the address transition detection signal delayed by the address transition detection signal delay circuit.

3. The boosting circuit as claimed in claim 1, wherein the first boosting means comprises:

a first PMOS transistor connected between the power supply terminal and a first node and driven by the potential of a second node;

a first NMOS transistor connected between the second node and the ground terminal and driven by the address transition detection signal;

a second PMOS transistor connected between the second node and the first node and driven by the address transition detection signal;

capacitors connected between the first node and the ground terminal and charged according to an inverted signal of the address transition detection signal; and

a second NMOS transistor connected between the capacitor and the ground terminal and driven by the address transition detection signal.

4. The boosting circuit as claimed in claim 1, wherein the sensing circuit comprises;

a PMOS transistor connected between the power supply terminal and the output terminal, wherein a gate terminal of the PMPS transistor is connected to the ground terminal;

a NMOS transistor connected between the output terminal and the ground terminal and driven by the reference voltage; and

a flash memory cell driven by the boosting voltage of the first boosting means.

5. The boosting circuit as claimed in claim 4, wherein the flash memory cell is an erase cell.

6. The boosting circuit as claimed in claim 1, wherein the switching circuit comprises:

a first switching means for outputting the boosting voltage of the first boosting means or a voltage of a Low level according to an inverted signal of the output signal of the sensing circuit;

a first PMOS transistor for applying the boosting voltage of the first boosting means according to the output signal of the first switching means;

a second switching means for outputting the boosting voltage of the first boosting means or a voltage of a Low level according to the output signal of the sensing circuit; and

a second PMOS transistor for applying the power supply voltage according to the output signal of the second switching means.

7. The boosting circuit as claimed in claim 1, wherein the second boosting means comprises:

a first PMOS transistor connected between the power supply terminal and the output terminal and driven by the potential of the first node;

a first NMOS transistor connected between the first node and the ground terminal and driven by the address transition detection signal;

a second PMOS transistor connected between the first node and the output terminal and driven by the address transition detection signal;

capacitors connected between the output terminal and the ground terminal and boosted by the boosting voltage of the first boosting means applied through the switching circuit or the power supply voltage; and

a second NMOS transistor connected between the capacitor and the ground terminal and driven by the address transition detection signal.